Abstract of the Disclosure

A method and apparatus are presented for on-chip testing of circuits in testing channels. In an embodiment of the present invention, the system includes a weight selector that allows for a wide variety of weighting of test data that is to be supplied to the testing channels. For example, the weight selector may be used to weight all bits in all channels or individual bits in a particular channel. Clock control and diagnostic logic may also be provided to selectively supply scan, functional, and/or stop clock signals to the testing channels. Channel filtering logic may be also provided to mask output data from a selected testing channel as desired. The method and apparatus may provide improved testing performance and power savings.